AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (original) A method for making a package structure with a cavity, comprising following steps:

providing a chip having a circuit disposed thereon and a plurality of first bonding pads disposed around the circuit;

providing a multi-layer ceramic substrate having a cave formed thereon and a plurality of second bonding pads disposed around the cave, wherein the cave and the plurality of second bonding pads are respectively corresponding to the circuit and the plurality of first bonding pads;

applying an adhesive layer to the surface of the substrate with the cave and the second pads exposed from the adhesive layer; and

tightly bonding the chip and the multi-layer ceramic substrate together such that the circuit of the chip is corresponding to the cave of the multi-layer ceramic substrate so as to form a cavity, and then electrically connecting the plurality of first bonding pads with the plurality of second bonding pads.

2. (original) The method as claimed in claim 1, wherein the plurality of first bonding pads are electrically connected to the plurality of second bonding pads by an ultrasonic bonding process.

3. (original) The method as claimed in claim 1, wherein the plurality of first bonding pads are electrically connected to the plurality of second bonding pads by a gold layer.

4. (original) The method as claimed in claim 1, wherein the chip is a SAW chip, and the circuit is an interdigital transducer (IDT).

5. (original) The method as claimed in claim 1, wherein the chip is a semiconductor chip.

6. (original) The method as claimed in claim 1, wherein the chip is an optical chip.

7. (original) The method as claimed in claim 1, wherein the chip is a crystal chip.

8. (original) The method as claimed in claim 1, wherein the chip is a MEMS chip.

9. (original) The method as claimed in claim 1, wherein the material of the multi-layer ceramic substrate is selected from a group of AlN, low-temperature co-fired ceramic (LTCC), multi-layer co-fired ceramic (MLCC), AL.sub.2O.sub.3, and polymeric materials.

10. (original) The method as claimed in claim 1 further comprising the step of sealing the upper portion of the chip and the multi-layer ceramic substrate with a buffer resin for stress relaxation and electrical insulation.

11. (original) The method as claimed in claim 10 further comprising the step of sealing the buffer resin with an exterior resin for mechanical protection and enhancement of moisture resistance.

12. (original) The method as claimed in claim 1, wherein a method for forming the

cave on the multi-layer ceramic substrate is mainly to punch a hole on at least first one green sheet from the top of a plurality of aligned green sheets before a sintering process for these green sheets, and then laminate these sheets, which include the green sheets with the hole thereon and green sheets without the hole thereon, so as to sinter these sheets to form the multi-layer ceramic substrate with the cave formed thereon.

13. (original) The method as claimed in claim 12, wherein the shape of the hole is square, rectangular, or oval.

14-16. (cancelled)